WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region, having an island shape, formed on the principal surface of said semiconductor substrate by introducing impurities of a second conductivity type by a plurality of ion implantation steps so as to have a smooth concentration profile in a depth direction of the semiconductor substrate;

a first conductivity type region formed inside said second conductivity type region by introducing impurities of the first conductivity type;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type region so as to reach at least said second conductivity type region on said first semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon filled in said trench with said insulation film interposed therebetween.

2. The semiconductor device according to claim 1, wherein said electrode portion is formed to have a T-shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the

semiconductor substrate.

3. A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region formed on the principal surface of said semiconductor substrate having an island shape by introducing impurities of a second conductivity type;

a highly doped first conductivity type region formed inside said second conductivity type region by introducing impurities of the first conductivity type at high concentration;

a plurality of first trenches each extending from a surface of said highly doped first conductivity type region so as to reach at least said second conductivity type region on said first semiconductor substrate;

an insulation film formed on an inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon filled in each of the first trenches with said insulation film interposed therebetween;

a plurality of second trenches formed inside said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches in parallel with said first trenches; and

a second conductivity type protrusion region

formed with a junction deeper than a junction of said second conductivity type region by introducing impurities of the second conductivity type through each of said second trenches by ion implantation.

4. The semiconductor device according to claim 3, wherein said electrode portion is formed to have a T-shaped cross section composed of a first part filling the trench and a second part protruding on the principal surface of the semiconductor substrate.

5. The semiconductor device according to claim 3, further comprising:

an electrode electrically connecting said highly doped first conductivity type region to said second conductivity type protrusion region through said second trench.

6. The semiconductor device according to claim 3, further comprising a portion of the second conductivity type region disposed between an adjacent pair of the first trenches, where the second trenches are not formed, wherein the portion is in an electrically floating state.

7. The semiconductor device according to claim 3, further comprising:

a first electrode provided in one of said second trenches for electrically connecting the second conductivity

type protrusion region to the highly doped first conductivity type region through the one of the second trenches;

second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the another one of the second trenches, the second electrode being disposed adjacent to the first electrode;

wherein one of adjacent pair of the first and second electrodes is in an electrically floating state.

8. The semiconductor device according to claim 5, further comprising a highly doped region contacting said electrode, and disposed between the electrode and the second conductivity type protrusion region.

9. The semiconductor device according to claim 5, wherein one of said plurality of first trenches encloses the portion of the second conductivity type region entirely.

10. The semiconductor device according to claim 3, wherein each of the first trenches is made shallower than each of the second conductivity type protrusion regions.

11. The semiconductor device according to claim 1, further comprising:

a plurality of electric field alleviating regions

formed by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region.

12. The semiconductor device according to claim 11, wherein each of the electric field alleviating regions is composed of:

a strip-wise third trench; and

a second conductivity type deep region formed through the strip-wise third trench.

13. The semiconductor device according to claim 11, wherein each of the electric field alleviating regions has a pn junction deeper than a pn junction of said second conductivity type region.

14. The semiconductor device according to claim 11, wherein said semiconductor device is constituted as a gate driving type power element for controlling a conduction state between a back surface of said semiconductor substrate and said first conductivity type region by using said electrode portion as a control electrode.

15. A method of manufacturing a semiconductor device comprising:

forming a second conductivity type region in a semiconductor substrate having a principal surface of a first

conductivity type by implanting impurities of a second conductivity type two or more times;

forming a first conductivity type region inside the island of said second conductivity type region, said first conductivity type region having a higher impurity concentration than said semiconductor substrate;

forming a trench in a depth direction of said semiconductor substrate by anisotropic etching;

forming a sacrificed oxide film on an inner wall surface of the trench by thermal oxidation;

removing said sacrificed oxide film;

forming an insulation film in an interior of said trench; and

filling said trench formed said insulation film with a polycrystalline silicon film.

16. The method of manufacturing a semiconductor device according to claim 15, further comprising, after the trench is filled with the polycrystalline silicon film:

patterning said film of polycrystalline silicon film so that the patterned polycrystalline silicon film has a T-shaped cross section with a wider width than an opening of said trench;

forming a highly doped first conductivity type region having a higher concentration than said first conductivity type region inside said first conductivity type region at a portion not coated by said polycrystalline silicon

film; and

forming a highly doped second conductivity type layer region inside said first conductivity type region formed at a region enclosed by two of said trenches.

17. The method of manufacturing a semiconductor device according to claim 15, wherein, said second conductivity type region is formed by performing ion implantation two or more times, and the each ion implantation of the impurities of the second conductivity type is carried out under a condition that acceleration energy is 200 keV or higher.

18. The method of manufacturing a semiconductor device according to claim 17, wherein, said second conductivity type region is formed by performing ion implantation two or more times, and said each ion implantation of the impurities is carried out under one of conditions that a dose is equal in the each ion implantation, and that a dose in the each ion implantation is smallest in ion implantation with lowest acceleration energy.

19. The method of manufacturing a semiconductor device according to claim 16, wherein said highly doped first conductivity type region is formed under a condition that a dose of implant ions is 1.0×10^{13} (atoms/cm^2) or less.

20. A method of manufacturing a semiconductor device

comprising:

forming a second conductivity type region in a semiconductor substrate having a principal surface of a first conductivity type;

forming a first conductivity type region inside said second conductivity type region, the first conductivity type region having a higher concentration than said semiconductor substrate;

forming a plurality of first trenches in a depth direction of said semiconductor substrate by anisotropic etching;

forming a sacrificed oxide film formed on an inner surface wall of each of the first trenches by thermal oxidation;

removing said sacrificed oxide film;

forming an insulation film in an interior of each of said first trenches;

filling each of the first trenches with a polycrystalline silicon film;

forming a plurality of second trenches in the second conductivity type region each positioned between an adjacent pair of said plurality of first trenches in parallel with said plurality of first trenches;

forming a second conductivity type protrusion region with a junction deeper than a junction of said second conductivity type region by introducing impurities of the second conductivity type from each of the second trenches by two or more ion implantation steps; and

forming a metal electrode so as to electrically connect said first conductivity type region with said second conductivity type protrusion region in each of the second trenches.

21. The method of manufacturing a semiconductor device according to claim 20, further comprising, after each of the first trenches is filled with the polycrystalline silicon film:

patterning said polycrystalline silicon film so that the patterned polycrystalline silicon film has a T-shaped cross section with a wider width than an opening of each of the first trenches;

forming a highly doped first conductivity type region inside said first conductivity type region at a portion from which said polycrystalline silicon film is removed, said highly doped first conductivity type region having a higher concentration than said first conductivity type region; and

forming a highly doped second conductivity type layer region inside said highly doped first conductivity type region at a portion between an adjacent two of said plurality of first trenches.

22. The method of manufacturing a semiconductor device according to claim 20, wherein at lest one of said ion implantation steps is carried out at acceleration energy of 200 keV or higher.

23. The method of manufacturing a semiconductor device according to claim 20, wherein at lest one of said ion implantation steps is carried out at acceleration energy of 30 keV or lower and a dose of implant ions at 1.0×10^{15} (atoms/cm^2) or more.

24. The method of manufacturing a semiconductor device according to claim 20, wherein the island of said second conductivity type region is formed by introducing impurities of a second conductivity type by two or more ion implantations.

25. The method of manufacturing a semiconductor device according to claim 15, further comprising:

forming a plurality of electric field alleviating regions by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region;

forming a plurality of strip-wise highly doped second conductivity type regions each formed inside each of the electric field alleviating regions;

forming a plurality of strip-wise third trenches each formed inside each of the strip-wise second conductivity type regions in a depth direction of said semiconductor substrate by anisotropic etching;

forming a plurality of deeper second conductivity type regions each formed inside each of said third trenches

by introducing impurities of the second conductivity type by two or more ion implantation steps;

forming a metal electrode which electrically connects each of said strip-wise second conductivity type region to each of said deeper second conductivity type region; and

forming a protection film at least on a surface of the semiconductor substrate except a region where said second conductivity type region underlies.

26. The method of manufacturing a semiconductor device according to claim 20, further comprising:

forming a plurality of electric field alleviating regions by introducing impurities of the second conductivity type in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region;

forming a plurality of strip-wise highly doped second conductivity type regions each formed inside each of the electric field alleviating regions;

forming a plurality of strip-wise third trenches each formed inside each of the strip-wise second conductivity type regions in a depth direction of said semiconductor substrate by anisotropic etching;

forming a plurality of deeper second conductivity type regions each formed inside each of said third trenches by introducing impurities of the second conductivity type by two or more ion implantation steps;

forming a metal electrode which electrically

connects each of said strip-wise second conductivity type region to each of said deeper second conductivity type region; and

forming a protection film at least on a surface of the semiconductor substrate except a region where said second conductivity type region underlies.

27. The method of manufacturing a semiconductor device according to claim 25, wherein each of said deeper second conductivity type region has a junction deeper than a junction of said second conductivity type region for forming a channel in a gate driving type power element having a high voltage withstanding characteristics.

28. The method of manufacturing a semiconductor device according to claim 26, wherein each of said deeper second conductivity type region has a junction deeper than a junction of said second conductivity type region for forming a channel in a gate driving type power element having a high voltage withstanding characteristics.